HIGH ISOLATION 1-20 GHZ MMIC SWITCHES WITH ON-CHIP DRIVERS

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ABSTRACT

MMIC SPST and SPDT reflective GaAs MESFET switches with on-chip TTL compatible drivers have achieved 50 dB isolation over the 1-20 GHz range. This is the highest isolation yet reported for MMIC switches covering this bandwidth. Insertion loss was less than 2.5 dB for the SPST switch and less than 2.7 dB for the SPDT switch. The MMIC switches were designed for convenient use and require only a single +12 volt power supply and external dc blocking capacitors. Switching time for either device was less than 15 nanoseconds. Good agreement was obtained between measured and simulated results.

INTRODUCTION

Broadband microwave switches are vital system building blocks. Previously reported MMIC switches [1]-[4] have not had sufficiently high isolation to be widely usable. This paper describes the design, fabrication and performance of MMIC SPST and SPDT switches with on-chip TTL compatible drivers. Both switch types cover 1-20 GHz, operate from a single +10 to +12 volt power supply and commute in less than 15 nanoseconds. Both have at least -12 dB return loss at all ports and handle +22 dBm signal levels. The SPST switch has an insertion loss of 2.5 dB and greater than 50 dB isolation. The SPDT switch insertion loss is 2.7 dB with 49 dB isolation. The switches are convenient to use, requiring only external dc blocking capacitors which set the lower end of their useful bandwidth. The excellent isolation achieved by these switches is principally attributable to the design of the series and shunt FETs used in their realization.

RF CIRCUIT DESIGN

The SPST and SPDT switches both make use of a single series FET switch and three distributed shunt switch FETs. Circuit diagrams of the RF portions of the SPST and SPDT devices are shown in Figure 1 and Figure 2, respectively.

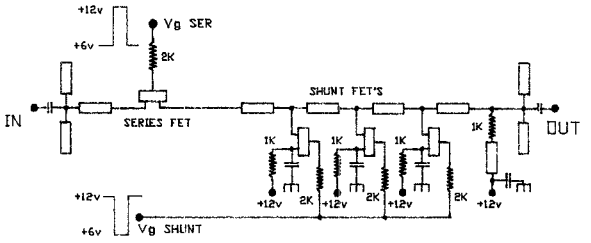

Figure 1. Simplified Schematic Diagram of SPST Switch without drivers. Input and output DC blocking capacitors are off chip.

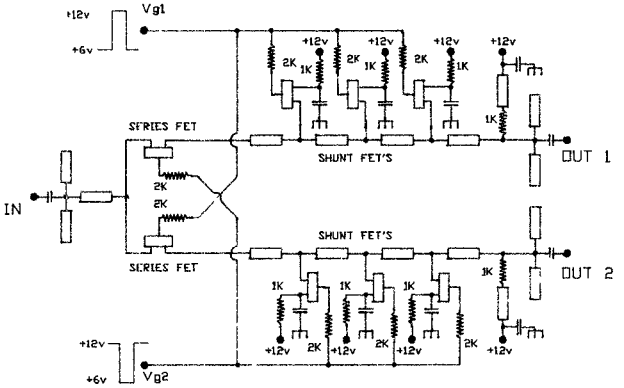

Figure 2. Simplified Schematic Diagram of SPDT Switch without drivers. Input and output DC blocking capacitors are off chip.

In order to operate from a single positive power supply, the drains and sources of all FETs are held at the +12V supply voltage. The FETs are switched from their low to high Rds state by application of +12 and +7V respectively to their gates. To obtain proper switching action, the series FET must be biased to the opposite state as the shunt FETs in the same switch arm. The sources

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of the shunt FETs are RF grounded through bypass capacitors so that they may be held at +12V. When the three shunt FETs are 'off', their Cds in concert with the series transmission lines form a matched low pass filter with a cutoff frequency well above 20 GHz. When the shunt FETs are 'on' they short circuit the series transmission line to ground at three locations. At the high end of the frequency range, spacing is such that isolation is readily obtained. At lower frequencies the shunt FETs behave as if they were in parallel reducing isolation. By placing a series FET ahead of the distributed shunt FETs, low frequency isolation is preserved. In the SPDT switch design, the 'off' arm adds a shunt capacitance which must be incorporated in the on path low pass filter structure. This approach accounts for the excellent on path VSWR of both switches. Each FET has a 2000 ohm GaAs resistor in series with its gate for RF isolation. Only minimal power is consumed during switching and speed is limited only by the 2K resistor-Cgs time constant (<1 nanosecond) and the driver. Great care was exercised in routing the FET gate control lines to prevent signal coupling from degrading isolation. A detailed linear simulation of each switch including all bias and control circuitry was performed. Distributed models were used for the series and shunt FETs and transmission line junction parasitics were accounted for. The results of the simulation are shown in Figure 3 for the SPST switch and in Figure 4 for the SPDT switch.

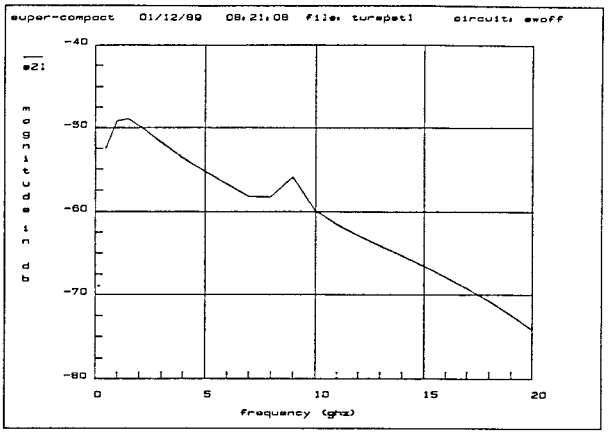

Figure 3a. Simulated SPST Switch Isolation using detailed switch model.

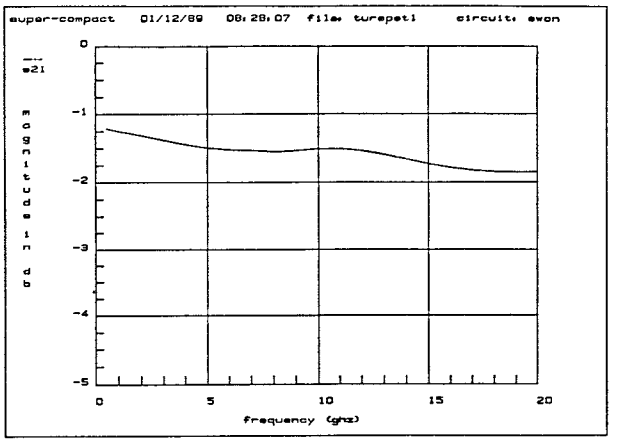

Figure 3b. Simulated insertion loss of SPST Switch calculated using detailed model.

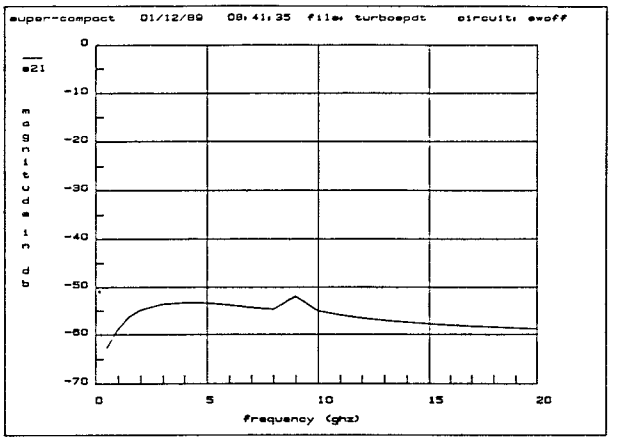

Figure 4a. Simulated SPDT Switch Isolation using detailed switch model.

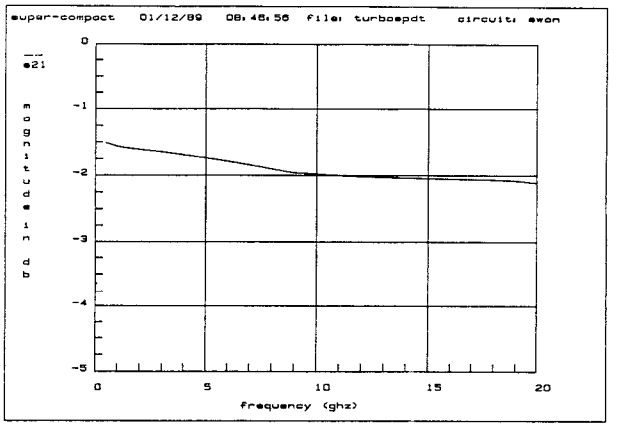

Figure 4b. Simulated insertion loss of SPDT Switch calculated using detailed model.

SWITCHING FET DESIGN

In order to obtain high isolation to 20 GHz attention must be given to minimizing the impedance to ground of the shunt FETs. This impedance is principally composed of the FET low field Rds in series with the reactance of elements between the FETs source and ground. Low field Rds may be minimized by using a large periphery FET. The upper limit on gate width is set by Coff (composed of Cds, Cgs and Cdg) which determines the cutoff frequency of the switch. By placing the shunt FETs on both sides of the signal path and using two via holes and a 25 pf MIM bypass capacitor on each source contact, source reactance to ground was also minimized. The structure of the shunt FET is shown in Figure 5.

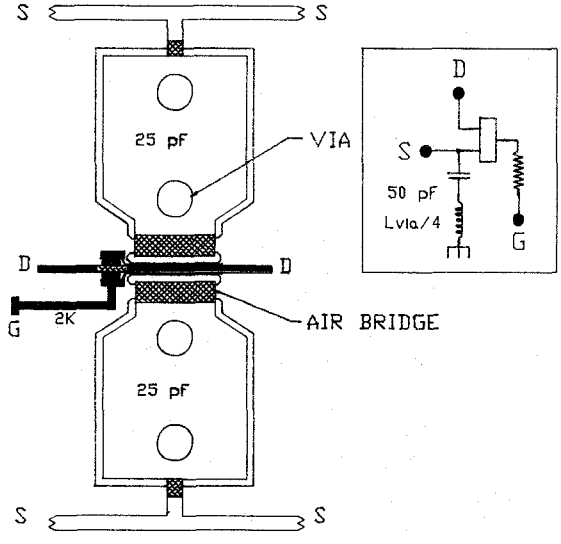

Figure 5. Shunt FET structure used in SPST and SPDT Switches. Note 25pf bypass capacitors on each source.

A distributed model for the shunt FET was derived by breaking the device into 6 lumped sections and properly locating the sections along the drain transmission line. The model given in Figure 6A uses the lumped section equivalent circuit shown in Figure 6B for the 'on' case and Figure 6C for the 'off' case.

The series FET was designed for low 'on' resistance to obtain low insertion loss. However; low 'on' resistance must be consistent with low enough Coff to provide at least 50 dB of isolation up to the frequency where the shunt FETs take over. The series FET structure was also designed to minimize parasitic capacitance to ground and is integrated into a high impedance microstrip line. The series FET illustrated in Figure 7 has sufficient periphery to handle +25 dBm.

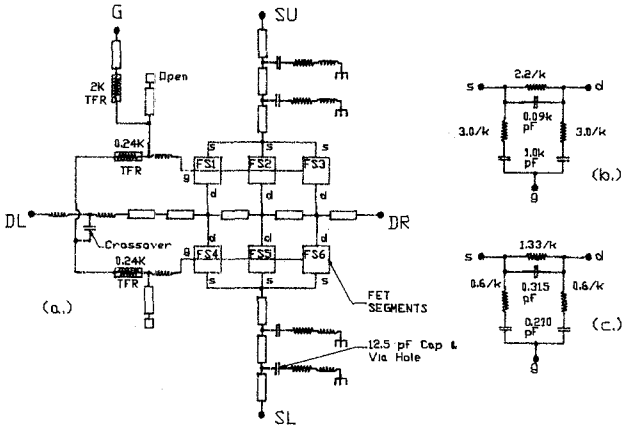

Figure 6. a. Distributed model of the shunt FET structure of Figure 5. The six FET segments are replaced by the circuits shown in Figures 6a. and 6b. in the 'on' and 'off' cases respectively. b. Model of FET segment in the 'on' state. c. Model of FET segment in the 'off' state. (k=Z/1000*6 where Z is the total FET periphery in microns).

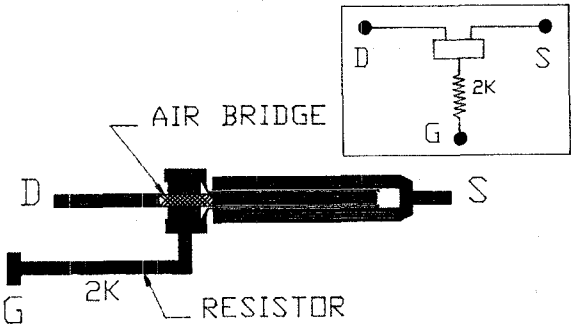

Figure 7. Series FET structure used in SPST and SPDT Switches. It is designed to minimize capacitance to ground.

DRIVER CIRCUIT DESIGN

The primary objectives of the on-chip driver circuit were to operate from a single positive supply voltage using minimal power, be compatible with TTL logic levels, achieve a 15 ns switching speed, and not affect chip size or yield unduly.

The circuit is a source-coupled Schmitt Trigger using depletion mode GaAs FETs [5]. Figure 8 shows a schematic diagram of the circuit. The circuit operates from a 0 - 5 volt transition applied at the input, and delivers +12 and approximately +6 volts at the FET control outputs. In addition, a complementary 0 - 5 volt output is provided for easy cascading in multi-pole applications. The driver circuit was simulated with Microwave SPICE, using FET models derived from DC I-V measurements

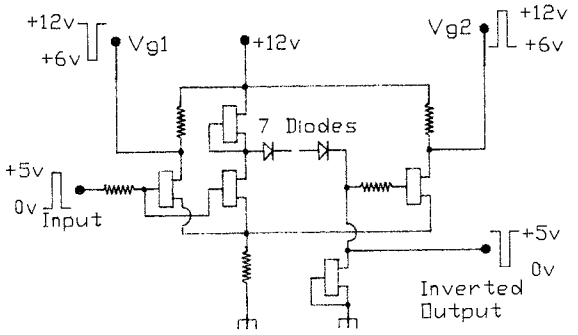

Figure 8. Driver Schematic Diagram

(non-linear model elements) and microwave S-parameter (linear parasitic model elements). Figure 9 shows the predicted time response of the driver circuit operating with a 24 MHz square wave as input.

In order to minimize the driver's impact on the total circuit yield, it was designed to tolerate wide variations in process parameters. The driver is predicted to operate properly over a +/- 30% variation in Idss and pinchoff voltage, a +/- 20% variation in resistor values, and four order-of-magnitude variation in diode Isat.

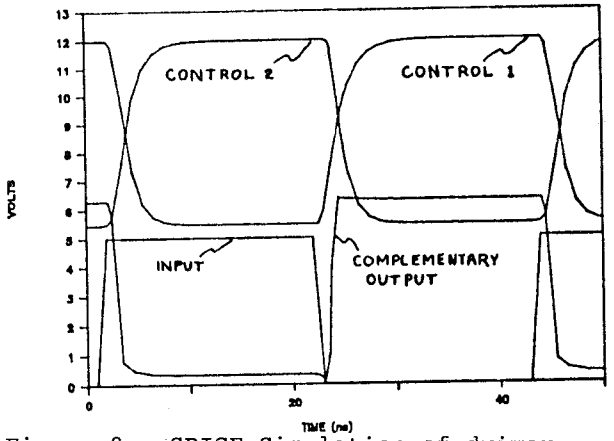

Figure 9. SPICE Simulation of driver circuit response to a 24 MHz square wave. Response includes effect of switch gate loading.

FABRICATION

These switches were fabricated at Texas Instruments using the standard 0.5 micron E-beam process and the "intermediate" doping profile. The intermediate profile is optimum for control applications due to its low sheet resistance (320 ohm/sq) resulting in low FET parasitic resistances. A very high yield capacitor process, including capacitors over via holes, allowed the realization of low inductance grounds necessary for 20 GHz isolation. Recent data taken at Texas Instruments shows no significant reliability degradation of capacitors fabricated over via holes.

MEASURED PERFORMANCE

The SPST and SPDT switches were measured in microstrip test fixtures containing 10 mil thick alumina substrates in 100 mil wide channels. The measured isolation of the empty fixtures was in excess of 70 dB. Switch characteristics were de-embedded from the measured data.

The insertion loss and isolation of the SPST switch is given in Figure 12. Maximum insertion loss is 2.5 dB and isolation is greater than 50 dB over the 1-20 GHz range. Return loss in the 'on' state is less than -12 dB at the input and -13 dB at the output. Power input for 1 dB compression was +22 dBm.

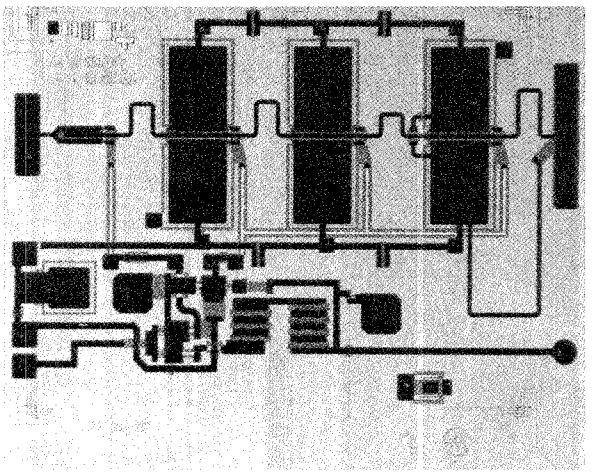

Figure 10. Photograph of SPST Switch. Chip size is 2.03x1.78 mm.

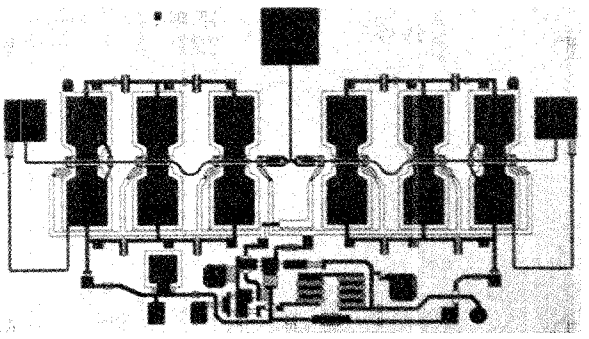

Figure 11. Photograph of SPDT Switch. Chip size is 3.40x1.78 mm.

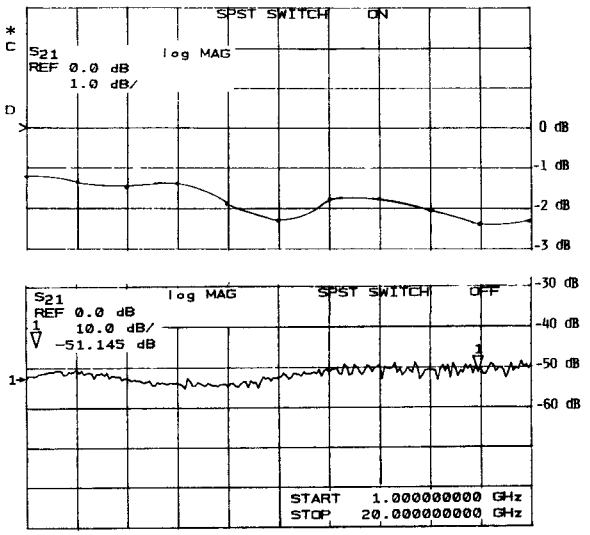

Figure 12. SPST Switch maintains 50dB isolation and less than 2.5 dB insertion loss over the 1-20 GHz frequency range.

Figure 13 gives the insertion loss and isolation of the SPDT switch. Over the 1-20 GHz range maximum insertion loss is 2.7 dB, minimum isolation is 49 dB. Return loss at any port is better than -12 dB. Power input for 1 dB compression was +21 dBm.

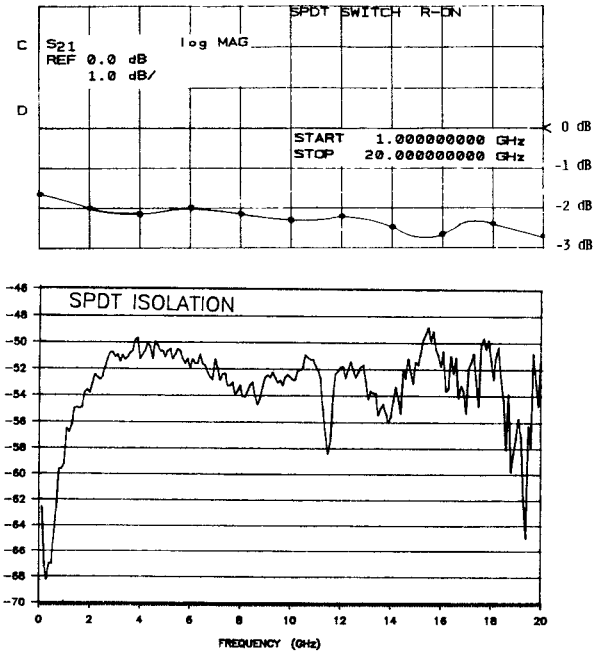

Figure 13. SPDT Switch provides 49 dB minimum isolation and less than 2.7 dB insertion loss acorss the 1-20 GHz bandwidth.

Both switches draw under 30 mA from the +12 V power supply and both functioned properly over a +8 to +12V supply voltage range. The switches required a low input level of 0.8 V or less and a high input level of 3.5 V or more to change state. The driver circuit provided at least 2 V of hysteresis for good noise immunity.

Compatibility with 54 F series TTL was demonstrated with measured switching times of under 13 nanoseconds for any transition of either switch.

CONCLUSION

MMIC SPST and SPDT reflective high isolation 1-20 GHz switches exhibiting isolations of 50 dB have been demonstrated. The switches contain on-chip TTL compatible drivers for ease of use. The SPDT chip contains 13 FETs and 7 diodes and thus reaches a level of integration where it is no longer a miniature MIC. The level of performance realized in these switches makes them ideal candidates for many system applications.

ACKNOWLEDGMENTS

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